Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-46 (Canceled).

Claim 47 (Original): A method of manufacturing a semiconductor device comprising:

forming a first gate electrode and a second gate electrode on a semiconductor substrate;

forming a diffusion layer, with the first gate electrode as a mask

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode, said second gate electrode and said diffusion layer in such a manner that a portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height equal to a height of said first gate electrode or above, another portion of said first insulating film is provided on a major part of said diffusion layer to a height lower than a height of said first gate electrode and a further portion of said first insulating film is provided on a minor part of said diffusion layer to a height equal to a height of said first gate electrode or above;

forming a second insulating film on said first insulating film;

forming a second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said diffusion layer, to form a contact hole leading to said major part of said diffusion layer; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said diffusion layer.

Claim 48 (Original): A method of manufacturing a semiconductor device comprising:

forming, on a semiconductor substrate, a plurality of first memory cell gates, a pair of first selecting gates sandwiching said first memory cell gates, a plurality of second memory cell gates and a pair of second selecting gates sandwiching said second memory cell gates;

forming a plurality of diffusion layers in said semiconductor substrate while using as masks said first memory cell gates, said pair of first selecting gates, said second memory cell gates and said pair of second selecting gates;

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first memory cell gates, said second memory cell gates and said diffusion layers in such a manner that portions of said first insulating film are embedded between said first memory cell gates and between said second memory cell gates, a portion of said first insulating film is provided on one of said diffusion layers, on which one of said pair of first selecting gates is adjacent to one of said pair of second selecting gates in such a manner that a part of said portion of said first insulating film, which is on a major part of said one of said diffusion layers, has a thickness thinner than a thickness of said portions of said first

insulating film, which are embedded between said first memory cell gates and between said second memory cell gates;

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said one of said diffusion layers, to form a contact hole leading to said major part of said one of said diffusion layers; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said one of said diffusion layers.